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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,197	08/27/2003	Li-Lien Lin	BHT-3212-39	3478

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EXAMINER	
CHAUDRY, MUJTABA M	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 06/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,197	LIN ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☒ Claim(s) *4,5 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-19 are presented for examination.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Oath/Declaration

The Oath filed August 27, 2003 complies with all the requirements set forth in MPEP 602 and therefore is accepted.

Drawings

The drawings filed August 27, 2003 are accepted.

Specification

The specification is objected to for the following informalities:

- A period is needed at the end of the sentence on page 3, line 16.
- The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors.

Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claim 4 is objected to because of the following informalities:

- A period should follow the termination of the claim.

Appropriate correction is required.

Claim 5 is objected to because of the following informalities:

- A period should follow the termination of the claim.

Appropriate correction is required.

Claim 7 is objected to because of the following informalities:

- A period should follow the termination of the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- It is not clear if the coding module is generating the variant correction code or the correcting module is calculating/generating the variant correction code. See lines 6-12 of claim 1. How does the correcting module store the variant correction code and then calculate it as well? Further, in claim 9, there is not antecedent for "said

variant identification error detection code" in lines 21-22. The claims are rejected based on guidance provided by MPEP 2111 and as written.

Appropriate correction is required.

Claims 5, 7 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- The claims recite generating a corresponding variant identification detection code via said identification coding process in advance. However, the claims do not state in advance to what, since advance is a relative term.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the

reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1, 2 and 8-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Williamson et al. (USPN 6615387).

As per claim 1, Williamson et al. (herein after: Williamson) teaches (abstract and Figure 8) an error correction and miscorrection detection apparatus includes a memory buffer for storing user data contained in a data signal. A syndrome computer circuit generates a plurality of EDC syndromes form an EDC codeword, which the Examiner would like to point out incorporates data along with parity (analogous to variant correction data, See col. 1, lines 38-60 and abstract). The EDC codeword includes user data encoded with a plurality of m-bit EDC parity symbols. The EDC codeword is encoded with plurality of n-bit ECC parity symbols to form the data signal, such that m>n. An ECC error correction circuit corrects the user data with an error signal generated for each corruption of the data signal. A completion is signal generated once correction of the EDC codeword is complete. A syndrome fix-up circuit (analogous to correcting module) is configured to adjust the EDC syndromes based on the received error signals. Once the completion signal is received, a miscorrection by the ECC error correction circuit is detected if a value of the adjusted syndromes is not equal to zero. See Figure 8:

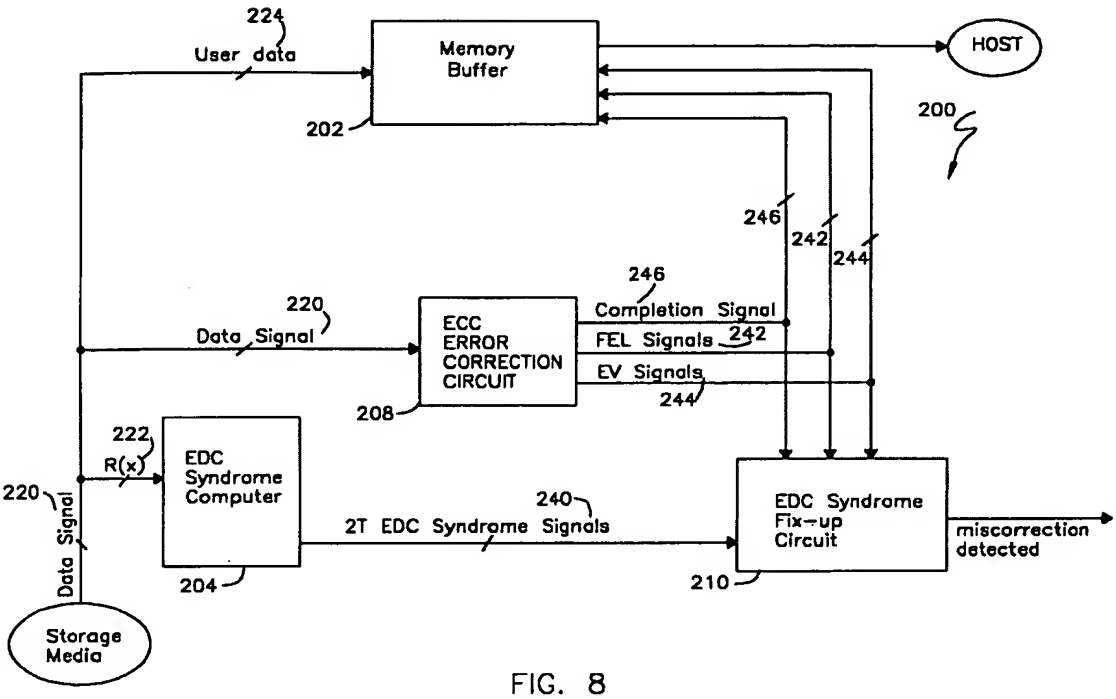

FIG. 8

As per claim 2, Williamson teaches (Figure 8) an EDC syndrome computer which is analogous to coding module of the present application. The Examiner would like to point out that the coding module is labeled as "computer" hence it is programmable. Even if it weren't, coding has to be performed by programming.

As per claim 8, Williamson teaches (col. 1, lines 19-60) linear block code is an error detection code.

As per claim 9, Williamson teaches (abstract and Figure 8) an error correction and miscorrection detection apparatus includes a memory buffer for storing user data contained in a data signal. A syndrome computer circuit generates a plurality of EDC syndromes form an EDC codeword, which the Examiner would like to point out incorporates data along with parity (analogous to variant correction data, See col. 1, lines 38-60 and abstract). The EDC codeword

includes user data encoded with a plurality of m-bit EDC parity symbols. The EDC codeword is encoded with plurality of n-bit ECC parity symbols to form the data signal, such that m>n. An ECC error correction circuit corrects the user data with an error signal generated for each corruption of the data signal. A completion is signal generated once correction of the EDC codeword is complete. A syndrome fix-up circuit (analogous to correcting module) is configured to adjust the EDC syndromes based on the received error signals. Once the completion signal is received, a miscorrection by the ECC error correction circuit is detected if a value of the adjusted syndromes is not equal to zero.

As per claim 10, Williamson teaches (Figure 8) an EDC syndrome computer which is analogous to coding module of the present application. The Examiner would like to point out that the coding module is labeled as "computer" hence it is programmable. Even if it weren't, coding has to be performed by programming.

As per claim 11, Williamson teaches (abstract and Figure 8) an error correction and miscorrection detection apparatus includes a memory buffer for storing user data contained in a data signal. A syndrome computer circuit generates a plurality of EDC syndromes form an EDC codeword, which the Examiner would like to point out incorporates data along with parity (analogous to variant correction data, See col. 1, lines 38-60 and abstract). The EDC codeword includes user data encoded with a plurality of m-bit EDC parity symbols. The EDC codeword is encoded with plurality of n-bit ECC parity symbols to form the data signal, such that m>n. An ECC error correction circuit corrects the user data with an error signal generated for each corruption of the data signal. A completion is signal generated once correction of the EDC codeword is complete. A syndrome fix-up circuit (analogous to correcting module) is configured

to adjust the EDC syndromes based on the received error signals. Once the completion signal is received, a miscorrection by the ECC error correction circuit is detected if a value of the adjusted syndromes is not equal to zero.

As per claim 12, Williamson teaches (col. 1, lines 19-60) linear block code is generated by coding original data.

As per claim 13, Williamson teaches (Figure 8) an EDC syndrome computer which is analogous to coding module of the present application. The Examiner would like to point out that the coding module is labeled as "computer" hence it is programmable. Even if it weren't, coding has to be performed by programming.

As per claim 14, Williamson teaches (col. 1, lines 19-60) linear block code is an error detection code.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3-7 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williamson et al. (USPN 6615387) further in view of Applicants Admitted Prior Art (AAPA).

As per claim 3, Williamson substantially teaches, in view of above rejections, (abstract and Figure 8) an error correction and miscorrection detection apparatus includes a memory buffer for storing user data contained in a data signal. A syndrome computer circuit generates a plurality of EDC syndromes form an EDC codeword, which the Examiner would like to point out incorporates data along with parity (analogous to variant correction data, See col. 1, lines 38-60 and abstract). The EDC codeword includes user data encoded with a plurality of m-bit EDC parity symbols. The EDC codeword is encoded with plurality of n-bit ECC parity symbols to form the data signal, such that m>n. An ECC error correction circuit corrects the user data with an error signal generated for each corruption of the data signal. A completion is signal generated once correction of the EDC codeword is complete. A syndrome fix-up circuit (analogous to correcting module) is configured to adjust the EDC syndromes based on the received error signals. Once the completion signal is received, a miscorrection by the ECC error correction circuit is detected if a value of the adjusted syndromes is not equal to zero.

Williamson does not explicitly teach the original data to comprise an identification data, EDC and main data as stated in the present application.

However, AAPA teaches (page 1, lines 14-21) original data to comprise an identification data, EDC and main data. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to format the original data of Williamson by to comprise an identification data, EDC and main data. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that by formatting the original data to comprise an identification data, EDC and main data would have reduced the

overall synchronization issues in coding and decoding processes since the length of each section would be well known in advance.

As per claim 4, AAPA substantially teaches, in view of above rejections, the identification error detection code is generated by coding the identification data. The Examiner would like to point out the EDC is usually generated on the data.

As per claim 5, Williamson substantially teaches, in view of above rejections, (Figure 8) to generate syndromes with the EDC syndrome computer.

As per claim 6, Williamson substantially teaches, in view of above rejections, (Figure 8) the EDC syndrome fix-up circuit which comprises XOR, also known to be used as comparators, for detecting errors.

As per claim 7, Williamson substantially teaches, in view of above rejections, (Figure 8) to generate syndromes from the variant correction data with the syndrome computer to form variant correction code, also known as EDC syndrome signals.

As per claim 15, Williamson substantially teaches, in view of above rejections, (abstract and Figure 8) an error correction and miscorrection detection apparatus includes a memory buffer for storing user data contained in a data signal. A syndrome computer circuit generates a plurality of EDC syndromes form an EDC codeword, which the Examiner would like to point out incorporates data along with parity (analogous to variant correction data, See col. 1, lines 38-60 and abstract). The EDC codeword includes user data encoded with a plurality of m-bit EDC parity symbols. The EDC codeword is encoded with plurality of n-bit ECC parity symbols to form the data signal, such that m>n. An ECC error correction circuit corrects the user data with an error signal generated for each corruption of the data signal. A completion is signal

generated once correction of the EDC codeword is complete. A syndrome fix-up circuit (analogous to correcting module) is configured to adjust the EDC syndromes based on the received error signals. Once the completion signal is received, a miscorrection by the ECC error correction circuit is detected if a value of the adjusted syndromes is not equal to zero.

Williamson does not explicitly teach the original data to comprise an identification data, EDC and main data as stated in the present application.

However, AAPA teaches (page 1, lines 14-21) original data to comprise an identification data, EDC and main data. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to format the original data of Williamson by to comprise an identification data, EDC and main data. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that by formatting the original data to comprise an identification data, EDC and main data would have reduced the overall synchronization issues in coding and decoding processes since the length of each section would be well known in advance.

As per claim 16, AAPA substantially teaches, in view of above rejections, the identification error detection code is generated by coding the identification data. The Examiner would like to point out the EDC is usually generated on the data.

As per claim 17, Williamson substantially teaches, in view of above rejections, (Figure 8) to generate syndromes with the EDC syndrome computer.

As per claim 18, Williamson substantially teaches, in view of above rejections, (Figure 8) the EDC syndrome fix-up circuit which comprises XOR, also known to be used as comparators, for detecting errors.

As per claim 19, Williamson substantially teaches, in view of above rejections, (Figure 8) to generate syndromes from the variant correction data with the syndrome computer to form variant correction code, also known as EDC syndrome signals.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts are included herein for Applicant's review.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mujtaba K. Chaudry whose telephone number is 571-272-3817. The examiner can normally be reached on Mon-Thur 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mujtaba Chaudry
Art Unit 2133
June 9, 2006

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